Exhibit A

# CYPRESS SEMICONDUCTOR

INTERNAL CORRESPONDENCE

DATE: Redacted WW:
TITLE: Data Retention & Window Margin
TO: Distribtuion
AUTHOR: Fred Jenne'
AUTHOR FILE: FRJ-
SUBJECT: SONOS, Data Retention
DISTRIBUTION: 1: YLY, SIM, IGK, BIP, LLO, JA

## I. Summary

We have erase data retention decay rate that is twice as large (120mv/decade) as we need (60mV/decade) to meet EOL conditions. We cannot meet EOL conditions with this decay rate of 120mV/decade.

The behavior of the erase decay rate was investigated by modifying the programming voltage and pulse width time to locate the offending injection mechanisms from the substrate or the gate. It was found that back streaming of electrons from the gate side is the apparent cause.

Experiments are defined at improving the quality of the dielectric from the standpoint of reducing the creation of trap sites both in the top blocking oxide and at the nitride/blocking oxide interface.

In addition other experiments are defined aimed at improving the window margin such as reducing VT shift with endurance, and increasing the effective field by reducing poly depletion.

## II. Discussion

The analysis by YLY shows that the erase decay rate is reduced from approximately 120mV/decade to about 60mV/decade if one does not erase the device deep into saturation. When operating in the saturation region there are electrons back streaming by FN conduction into the nitride layer annihilating the holes. When this occurs three things happen to a larger or smaller extent.

First traps are created in the blocking oxide increasing the conductivity of the film by trap assisted tunneling.

Second the high energy FN electrons damage the nitride layer creating low energy trap sites. In addition when the electrons annihilate the trapped holes additional damage occurs.

Thirdly the electrons can create trap sites at the blocking oxide/nitride interface.

If the damage in the nitride film results in low energy trap sites, then the charge will be thermally emitted at a much higher rate for a given temperature and therefore significantly increase the decay rate.

**A. Annealing**

If the deposited blocking oxide and its interface to the nitride layer is not fully annealed, then both will have a high number trap sites. The annealing (meaning elimination of Si dangling bonds, Si micro-clusters, and dangling bonds at the oxide/nitride interface) we presently do is not as robust as others have reported in the industry.

The hypothesis is if we robustly anneal the blocking oxide and form a uniform terminated interface at the oxide nitride interface then we will see a reduction in the erase decay rate.

Another area of concern is that the resist strip after ONO etch. It is a plasma strip that distills what ever is in the resist down to the surface of the un-densified (un-annealed) blocking oxide that has un-terminated bonds that will link to what ever has been distilled out, and in addition any contamination like Na will easily diffuse deep into the film to the interface (Plasma wafer temperature about 150°C).

Hypothesis is if we robustly anneal the blocking oxide and use a chemical strip the erase decay rate will be improved.

**B. Deuterium Nitride**

Deuterium anneal of gate oxides have shown to improve the HEI reliability. This has been attributed to the deuterium bonds being harder to break than hydrogen thereby resulting in lower trap generation. I believe that using nitride deposited using ND3 (deuterium) will result in a superior SONOS device with better data retention and smaller endurance threshold shift. In addition I believe that depositing the SAC nitride using ND3 (deuterium

source) will result in a better annealed technology with higher CMOS HEI immunity. More on this later.

Hypothesis is using ND3 to deposit the memory nitride layer will resulting a SONOS device with improved data retention and smaller endurance threshold shift.

## III. Other Margin Factors

The shift in threshold due to endurance cycling is a direct offset adding to the window margin. Experimental evidence indicates that when processed with resist on the un-densified blocking oxide a larger threshold shifts results relative to the no-resist split. This indicates that the resist is contaminating the un-densified blocking oxide as described previously.

Hypothesis is annealing the blocking oxide and or using a chemical resist strip will result in a smaller threshold shift with endurance cycling.

Poly depletion reduces programming window for a given voltage. The poly depletion region effectively makes the stack thicker, which reduces the bias across the ONO stack. The poly depletion is a function of the poly doping, energy, and thermal history.

Hypothesis is by increasing the poly doping at the poly/oxide interface will improve the window margin.

A recent paper by Sandia indicates that nitriding the tunnel oxide significantly reduces the endurance cycling threshold shift. This would be another variable to investigate.

## IV. Experiment

Blocking Oxide Anneal/Densification: Improve data retention & reduce Vt endurance shift.

- 900C Steam 30'
- Anneal in $N_2O$

Effect of Thicker BO: Improve data retention & reduce endurance Vt shift.

- Analyze by across wafer variation

Nitridizing Tunnel Oxide: Reduce endurance Vt shift.

- Anneal tunnel oxide using $N_2O$

Depositing Deuterated nitride layer: Improve data retention and reduce endurance Vt shift.

Reduce Poly Depletion: Improve window margin.

- Increase poly doping, and or energy
- Optimize thermal history (Example 1,000°C RTA for 10' to produce higher activation of P dopant)

Reduce BO Contamination: Improve Window Margin & Data Retention.

- Pre-anneal blocking oxide before resist.
- Remove Tunnel oxide resist with chemical strip.

## V. Experimental Matrices

The matrices shown below roughly define the experiments to address the above hypothesizes.

| | LOT 752 16 Wafers | Anneal | | |
|---|---|---|---|---|
| | | Base line | 900C H2O | N2O |
| ONO | Base Line | 2 | 2 | 2 |
| | Tunnox N2O | 2 | 2 | 2 |
| | AVP | 2 | 2 | |

**Horizontal ONO**

| LOT 796 12 Wafers | Anneal | | | |
|---|---|---|---|---|
| | 900C H2O | | Base Line | |
| Resist | 2 | 2 | 2 | 2 |
| W/O Resist | | 2 | | 2 |
| | Wet | Plasma | Wet | Plasma |
| | Resist Strip | | | |

**AVP ONO**

| | LOT 796 8 Wafers | Poly Dose | | | |
|---|---|---|---|---|---|
| | | 1.00E+16 | | 5.50E+16 | |
| RTA Anneal | Base Line | 2 | 2 | 2 | 2 |
| | 1,000C 10' | | 2 | 2 | |
| | | 75KEV | 50KEV | 75KEV | 50KEV |
| | | Energy | | | |

| | LOT X 16 Wafers | TIP Energy | | | |
|---|---|---|---|---|---|
| | | Base Line | 50KEV | | |
| DEPI Dose | 4.50E+12 | 2 | 2 | Base Line | NCHI Energy |
| | | 2 | 2 | Add 20% | |
| | 4.00E+12 | 2 | 2 | Base Line | |
| | | 2 | 2 | Add 20% | |
| | | Base Line | 60KEV | | |
| | | DEPI Energy | | | |

PATENT
5298-08101/PM01039D

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:
Ramkumar et al.

Serial No.: 10/740,205

Filed: December 18, 2003

For: SONOS STRUCTURE INCLUDING A DEUTEREATED OXIDE-SILICON INTERFACE AND METHOD FOR MAKING THE SAME

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Group Art Unit: 2814

Examiner: Pham, H.

Atty. Dkt. No.: 5298-08101

I hereby certify that this correspondence is being transmitted via facsimile or deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313, on the date indicated below:

May 23, 2005
Date

Kevin L. Daffer

**DECLARATION UNDER 37 C.F.R. § 1.131**

Commissioner for Patents
Washington, D.C. 20231

I, Frederick B. Jenne, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 10/740,205 filed on December 18, 2003, a divisional application of parent U.S. Patent Application No. 10/094,108 filed on May 8, 2002.

2. I have been informed that in the present application certain claims have been rejected in reference to U.S. Patent No. 6,661,065 to Kumikiyo, which was issued on December 9, 2003, was first published on April 25, 2002, and was filed on February 13, 2001.

## CONCEPTION

3. As supported below, I, along with Krishnaswamy Ramkumar, conceived of the subject matter claimed in the present application within the United States before February 13, 2001. The subject matter includes a semiconductor topography including a silicon-oxide-nitride-oxide-silicon (SONOS) structure and a nitride layer comprising deuterium arranged above the SONOS structure.

4. Exhibit A attached hereto is a true copy of a memorandum which bears a date before February 13, 2001 corresponding to the conception of the invention. The actual date of the memorandum has been redacted.

5. Pages 2 and 3 of Exhibit A describe the subject matter of the presently claimed case including a semiconductor topography with a SONOS structure having a nitride layer formed using deuterium and a SAC (self aligned contact) nitride layer formed using deuterium.

## REDUCTION TO PRACTICE AND DILIGENCE

6. From at least a time just prior to February 13, 2001 through the filing of parent U.S. Patent Application No. 10/094,108 filed on May 8, 2002, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley Rose, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to February 13, 2001 through the filing of the parent application on May 8, 2002.

7. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to February 13, 2001 through the filing of the parent application on May 8, 2002.

8. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these

statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Frederick B. Jenne

Date: 4/11/05